REMARKS

Applicants appreciate the thoroughness with which the Examiner has examined the above-identified application. Reconsideration is requested in view of the amendments above and the remarks below.

Allowable claims

Applicants note that claims 5, 12, 14, 16 and 18 have been indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. Accordingly, new independent claim 19 combines the subject matter of claims 1, 2 and 5; new independent claim 20 combines the subject matter of claims 11 and 12; new independent claim 21 combines the subject matter of claims 11, 13 and 14; new independent claim 22 combines the subject matter of claims 15 and 16; new independent claim 23 combines the subject matter of claims 15, 17 and 18. Claims 5, 12, 14, 16 and 18 have been consequently cancelled.

Claim amendments

Claim 9 has been amended to recite a "parallel computing" memory structure, in accordance with the amendment made previously to claim 1.

Rejection under 35 USC § 103

Claims 1-4, 6-9 and 10 stand rejected under 35 USC § 103 as being obvious from Meyer U.S. Patent No. 6,397,299 in view of Cai et al. U.S. Patent Publication No. US2001/0049770A1 and, apparently, Kinoshita et al. U.S. Patent No. 4,703,422. Applicants respectfully traverse this rejection.

Claims 1 and 9

Applicants' invention as defined in claims 1-4 and 9 is directed to a computer program storage device containing a computer-readable program having a memory structure for parallel computing (claims 1-4) and a computer program product for parallel computing having computer code defining computer memory structure (claim 9). The parallel computing memory structure has first and second levels of hierarchy. The first level comprises a plane containing a thread which represents an independent flow of control managed by a program structure, heap and stack portions, and local variables and global data accessible by the program structure. The second level comprises a space containing two or more of the planes, wherein the planes in the space contain the program structure. The space also contains common data accessible by the program structure between each of the planes. As stated in the specification at page 10, lines 17-21, the invention naturally enables the design and implementation of parallel algorithms with minimal and well defined data space interaction, thus providing low cost, high performance parallelism without necessitating the programmer being an expert in the management of parallelism.

Unlike applicants' claimed program-based parallel computing memory structure, the primary reference Meyer patent is directed to a method of using non-cacheable memory that is physically distinct from main memory, and appears to use different speed memory for faster access. Meyer never even mentions parallel computing or processing, and does not teach or suggest applicants' parallel computing memory structure having the claimed first and second levels of hierarchy, and detailed structure therein. Since

applicant's invention is described as a "parallel computing memory structure" (and not merely a preamble recitation), Meyer, as the primary reference, represents non-analogous art with which one of ordinary skill in the art would not begin to construct a parallel computing memory structure. *See, Rowe v. Dror*, 112 F.3d 473, 42 USPQ2d 1550, 1553-55 (Fed. Cir. 1997) (PTO erred in rejecting claim with preamble "balloon angioplasty catheter" in preamble on basis of prior art reference that showed general purpose balloon catheter and made no suggestion as to suitability for angioplasty procedures). Moreover, there is no suggestion in Meyer to combine it with the secondary Cai reference.

Cai is directed to a buffer memory management in a system having multiple execution entities. While Cai makes mention that "the multi-unit data cache system may offer high access bandwidth by increasing parallelism for a multithreading or multitasking processor" (paragraph 0053), the structure of the cache or buffer memories is not comparable to that of applicants' claimed parallel computing memory structure with first and second levels of hierarchy having the recited features. For example, applicants' first level of hierarchy comprises a plane containing a thread which represents an independent flow of control managed by a program structure, and the second level of hierarchy comprises a space containing two or more of said planes. This structure is simply not disclosed or suggested by Cai's buffer memory structure, or the "program execution entity, such as a ... thread" (paragraph 0005).

The Examiner previously acknowledged that Meyer and Cai separately or in combination do not teach forming another level of hierarchy. See October 31, 2003 Office action, p.6. The Kinoshita patent has now been cited to for its disclosure in its

Abstract and at column 1, lines 52-55 relating to "hierarchy storages" in computer memory. However, Kinoshita's memory hierarchy also has nothing to do with parallel computer memory structure, and makes no suggestion of applicant's claimed first level of hierarchy which comprises a plane containing a thread representing an independent flow of control managed by a program structure, and second level of hierarchy comprising a space containing two or more of said planes. Accordingly, the combination of Meyer , Cai and Kinoshita does not make obvious applicant's claims 1 and 9.

Claims 2-4, 6-8 and 10

Applicants' claims 2-4, 6-8 and 10 add to the previously described parallel computing memory structure a third level of hierarchy comprising two or more of the spaces containing the same or different program structures having a library of programs, and common data accessible by the program structure between each of the spaces. Again, Meyer , Cai and Kinoshita do not individually or in combination suggest the combination of the claimed three levels of hierarchy in a parallel computing memory structure to render claims 2, -4, 6-8 and 10 obvious to one of ordinary skill in this art.

Claims 11 and 15

Claim 11 is directed to a method of parallel processing which uses the memory structure as described in claim 1, and adds the steps of employing first and second threads managed by the program structure to access the specified data in first and second planes, while the threads avoid interaction except when explicitly requested by the program structure. Claim 15 is directed to a program storage device that uses the memory structure as described in claim 1, and the method steps as described in claim 11.

The hypothetical combination of the non-analogous Meyer patent with Cai and Kinoshita again does not disclose or suggest applicants' claimed memory structure used in its parallel processing method, as discussed above. The EIDs that the Examiner references in the Cai patent are not disclosed as having the same properties as the threads in applicants' claims 11 and 15, where the first thread operates in the first plane of the first level hierarchy, and the second thread operates in the space (i.e., two or more planes) of the second level hierarchy, wherein the first and second threads only interact when explicitly requested by the program structure. Cai's EIDs are not disclosed as operating separately on different hierarchy levels, as applicants claim, and therefore the combination of Meyer, Cai and Kinoshita cannot render applicants' invention obvious.

Claims 13 and 17

Claims 13 and 17 add to base claims 11 and 15, respectively, the provision of the third level of hierarchy and the step of accessing the common data between each of said spaces by said first and second threads, and is not obvious from a hypothetical combination of Meyer, Cai and Kinoshita for the reasons given in connection with claims 2-4, 6-8 and 10, discussed above.

It is respectfully submitted that the application has now been brought into a condition where allowance of the entire case is proper. Reconsideration and issuance of a notice of allowance are respectfully solicited.

Respectfully submitted,

Peter W. Peterson
Reg. No. 31,867

DeLIO & PETERSON, LLC
121 Whitney Avenue
New Haven, CT 06510-1241
(203) 787-0595

ibmf100273000amdB.doc